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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,471	01/29/2004	Takeshi Morita	2004_0135A	3718

513 7590 05/18/2005

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,471	MORITA, TAKESHI	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-10,14,15,19 and 20* is/are rejected.

7)☒ Claim(s) *11-13 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: line 6 the claim reads "patters", however it should read "patterns". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 9 and 14 and their dependent claims are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claims 1 and 14, the claims disclose that the dummy patterns are formed in "*standard areas*", however these areas are not supported by Applicant's specification. Regarding claim 9 and 14, the claims disclose "*standard areas arranged in a matrix with predetermined spacing*", however this arrangement is not supported by Applicant's specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Motoyama et al. (U.S. Patent No. 6,099,992). With regard to Claim 1, Motoyama discloses a semiconductor device comprising:

a semiconductor substrate (31) having a pattern forming region which is the region containing interconnection layers (34a, 34b, 34c) as disclosed on figure 9E and a pattern non-forming region which is the region containing dummy patterns (35a, 35b, 35c) also disclosed on figure 9E

a wiring pattern comprising said interconnection layers (34a, 34b, 34c) formed on said pattern forming region;

a plurality of said dummy patterns (35a, 35b, 35c) formed on said pattern non-forming region;

an insulating film (36) formed on said wiring pattern and said plurality of dummy patterns (35a, 35b, 35c) as disclosed on figure 9F;

wherein each of said plurality dummy patterns (35a, 35b, 35c) is spaced apart with a width filled by plus sizing of said insulating film (36) formed on said plurality of dummy patterns, also disclosed on figure 9F.

It is noted that the claimed "*standard areas*" are not supported by Applicant's disclosure and thus the limitation was not given patentable weight.

With regard to Claim 6, Motoyama discloses a lattice-like pattern that superposed on the dummy patterns to form divided and mutually separated groups of dummy patterns, thus the reference discloses the claimed dummy patterns arranged in lattice form. It is noted that the claimed "*standard areas*" are not supported by Applicant's disclosure and thus the limitation was not given patentable weight.

With regard to Claim 14, Motoyama discloses a semiconductor device comprising:

a semiconductor substrate (31) having a pattern area which is the area containing interconnection layers (34a, 34b, 34c) as disclosed on figure 9E and a non-pattern area which is the area containing dummy patterns (35a, 35b, 35c) also disclosed on figure 9E

a conductor pattern comprising said interconnection layers (34a, 34b, 34c) formed on said pattern area;

a plurality of said dummy patterns (35a, 35b, 35c) formed on said non-pattern area of said semiconductor substrate (31).

It is noted that the claimed limitations "*wherein each of said plurality of dummy patterns are formed in a plurality of standard areas being arranged in a matrix with predetermined spacing; and wherein each of said plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of said semiconductor device is reduced*", are not supported by Applicant's disclosure and thus the limitations were not given patentable weight.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 7-10, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoyama (U.S. Patent No. 6,099,992). With regard to Claim 5, figures 9E and 9F disclose dummy pattern (35b) having a square shape, however the figures fail to disclose that each of the dummy patterns has a square shape. It would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure disclosed by Motoyama to include each of the dummy patterns has a square shape, as claimed, in order to optimize the size occupied by the dummy patterns and thus optimize also the device size. It is noted that the claimed "*standard areas*" are not supported by Applicant's disclosure and thus the limitation was not given patentable weight.

With regard to Claims 7 and 20, a further difference between the claimed invention and the structure disclosed on figures 9E and 9F is, the claimed width of approximately less than 72 μm would have been obvious to one having ordinary skill in the art at the time of the invention, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). In the instant case, such a modification would be done in order to optimize the size of the device.

With regard to Claims 8 and 19, a further difference between the claimed invention and the structure disclosed on figures 9E and 9F is, the claimed dummy patterns being line patterns. It would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure disclosed by Motoyama to include the claimed dummy patterns being line patterns, as claimed, in order to optimize the size occupied by the dummy patterns and thus optimize also the device size.

With regard to Claim 9, Motoyama discloses a semiconductor device comprising:

a semiconductor substrate (31) having a pattern area which is the area containing interconnection layers (34a, 34b, 34c) as disclosed on figure 9E and a non-pattern area which is the area containing dummy patterns (35a, 35b, 35c) also disclosed on figure 9E

a conductor pattern comprising said interconnection layers (34a, 34b, 34c) formed on said pattern area;

a plurality of said dummy patterns (35a, 35b, 35c) formed on said non-pattern area of said semiconductor substrate (31).

It is noted that the claimed limitations "*each of said plurality of dummy patterns having a standard rectangular outline and being arranged in a matrix with predetermined spacing; and wherein each of said plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of said semiconductor device is reduced*", are not supported by Applicant's disclosure and thus the limitations were not given patentable weight.

With regard to Claim 10, figures 9E and 9F disclose dummy pattern (35b) having a square outline, however the figures fail to disclose that each of the dummy patterns has a square outline. It would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure disclosed by Motoyama to include each of the dummy patterns has a square outline, as claimed, in order to optimize the size occupied by the dummy patterns and thus optimize also the device size. It is noted that the claimed "*standard areas*" are not supported by Applicant's disclosure and thus the limitation was not given patentable weight.

Allowable Subject Matter

5. Claims 11-13 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 5-20 have been considered but are moot in view of the new ground(s) of rejection and the comments relating to the subject matter not supported by Applicant's disclosure.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
5/15/05

TOM THOMAS
SUPERVISORY PATENT EXAMINER